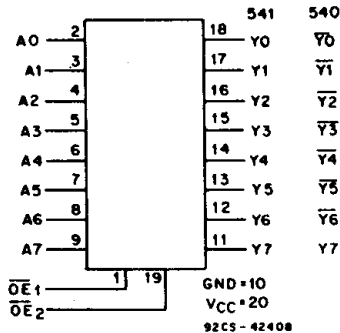


CD54/74AC540, CD54/74AC541 CD54/74ACT540, CD54/74ACT541



Data sheet acquired from Harris Semiconductor
SCHS285A – Revised November 1999



Octal Buffer/Line Drivers, 3-State

CD74AC/ACT540 - Inverting
CD74AC/ACT541 - Non-Inverting

Type Features:

- Buffered inputs
- Typical propagation delay:
4.5 ns @ $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 50 pF$

Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST®/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply.
- ± 24 -mA output drive current
 - Fanout to 15 FAST® ICs
 - Drives 50-ohm transmission lines

®FAST is a Registered Trademark of Fairchild Semiconductor Corp.

The CD54/74AC540, -541, and CD54/74ACT540, -541 octal buffer/line drivers use the RCA ADVANCED CMOS technology. The CD54/74AC/ACT540 are inverting 3-state buffers having two active-LOW output enables. The CD54/74AC/ACT541 are non-inverting 3-state buffers having two active-LOW output enables.

The CD74AC540, -541, and CD74ACT540, -541 are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Industrial (-40 to +85°C) and Extended Industrial/Military (-55 to +125°C).

The CD54AC540, -541, and CD54ACT540, -541, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.

TRUTH TABLE

CD54/74AC/ACT540		
INPUTS		OUTPUTS
OE1, OE2	A	Y
L	L	H
L	H	L
H	X	Z

TRUTH TABLE

CD54/74AC/ACT541		
INPUTS		OUTPUTS
OE1, OE2	A	Y
L	L	L
L	H	H
H	X	Z

H = High Voltage
L = Low Voltage
X = Immaterial
Z = High Impedance

CD54/74AC540, CD54/74AC541 CD54/74ACT540, CD54/74ACT541

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (V_{CC})	-0.5 to 6 V
DC INPUT DIODE CURRENT, I_{IK} (for $V_I < -0.5$ or $V_I > V_{CC} + 0.5$ V)	± 20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (for $V_O < -0.5$ or $V_O > V_{CC} + 0.5$ V)	± 50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I_O (for $V_O > -0.5$ or $V_O < V_{CC} + 0.5$ V)	± 50 mA
DC V_{CC} OR GROUND CURRENT (I_{CC} or I_{GND})	± 100 mA*
PACKAGE THERMAL IMPEDANCE, θ_{JA} (see Note 1): E package	69°C/W
M package	58°C/W
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):		
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s maximum	+265°C
Unit inserted into PC board min. thickness $1/16$ in. (1.59 mm) with solder contacting lead tips only	+300°C

* For up to 4 outputs per device: add ± 25 mA for each additional output.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

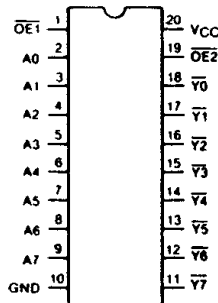
RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

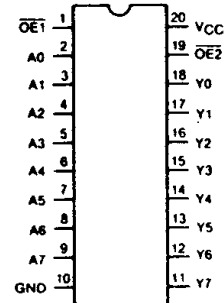
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC} *: (For T_A = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V_i, V_o	0	V_{CC}	V
Operating Temperature, T_A :	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

*Unless otherwise specified, all voltages are referenced to ground.

TERMINAL ASSIGNMENT DIAGRAMS



CD54/74AC/ACT540



CD54/74AC/ACT541

Technical Data

CD54/74AC540, CD54/74AC541 CD54/74ACT540, CD54/74ACT541

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS	
				+25		-40 to +85		-55 to +125			
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage V _{IH}			1.5	1.2	—	1.2	—	1.2	—	V	
			3	2.1	—	2.1	—	2.1	—		
			5.5	3.85	—	3.85	—	3.85	—		
Low-Level Input Voltage V _{IL}			1.5	—	0.3	—	0.3	—	0.3	V	
			3	—	0.9	—	0.9	—	0.9		
			5.5	—	1.65	—	1.65	—	1.65		
High-Level Output Voltage V _{OH}	V _{IH} or V _{IL}	#, *	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
Low-Level Output Voltage V _{OL}	V _{IH} or V _{IL}	#, *	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
Input Leakage Current I _I	V _{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND		5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI I _{CC}	V _{CC} or GND	0	5.5	—	8	—	80	—	160	μA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

Technical Data

CD54/74AC540, CD54/74AC541 CD54/74ACT540, CD54/74ACT541

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS	
				+25		-40 to +85		-55 to +125			
	V _I (V)	I _O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V _{IH}		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V _{IL}		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	V _{OZH}	V _{IH} or V _{IL} #, *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V _{OL}	V _{IH} or V _{IL} #, *	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I _I	V _{CC} or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I _{CC}	V _{CC} or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI _{CC}	V _{CC} -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*	
	540	541
DATA	1.42	0.5
OE1, OE2	1.3	1.3

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Technical Data

CD54/74AC540, CD54/74AC541
CD54/74ACT540, CD54/74ACT541

SWITCHING CHARACTERISTICS: AC Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Output AC540	t_{PLH}	1.5	—	77	—	85	ns
	t_{PHL}	3.3*	2.4	8.6	2.4	9.5	
AC541		5†	1.8	6.2	1.7	6.8	
Enable, to Output to Output	t_{PLH}	1.5	—	89	—	98	ns
	t_{PHL}	3.3	2.8	9.9	2.7	10.9	
		5	2.1	7.1	2	7.8	
Disable to Output to Output	t_{PZL}	1.5	—	136	—	150	ns
	t_{PZH}	3.3	4.6	16.4	4.5	18	
		5	3.1	10.9	3	12	
Power Dissipation Capacitance AC540 AC541	$C_{PD}‡$	—	60 Typ.		60 Typ.		pF
		—	60 Typ.		60 Typ.		
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_i	—	—	10	—	10	pF
3-State Output Capacitance	C_o	—	—	15	—	15	pF

SWITCHING CHARACTERISTICS: ACT Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Data to Output ACT540	t_{PLH}	5†	1.9	6.5	1.8	7.2	ns
	t_{PHL}						
ACT541							
Enable to Output	t_{PLH}	5†	2.1	7.5	2.1	8.2	ns
	t_{PHL}						
Disable to Output	t_{PZL}	5	3.5	12.2	3.4	13.4	ns
	t_{PZH}						
Power Dissipation Capacitance ACT540 ACT541	$C_{PD}§$	—	60 Typ.		60 Typ.		pF
		—	60 Typ.		60 Typ.		
Min. (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C_i	—	—	10	—	10	pF
3-State Output Capacitance	C_o	—	—	15	—	15	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

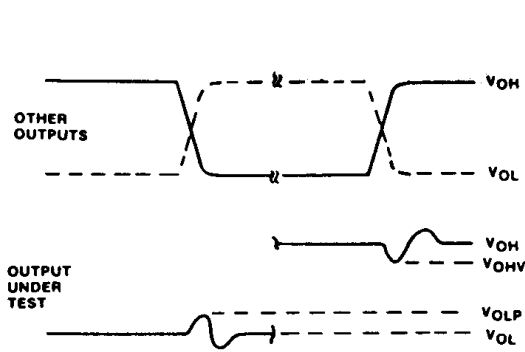
§ C_{PD} is used to determine the dynamic power consumption, per channel.

For AC series, $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

For ACT series, $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
 C_L = output load capacitance
 V_{CC} = supply voltage.

CD54/74AC540, CD54/74AC541 CD54/74ACT540, CD54/74ACT541

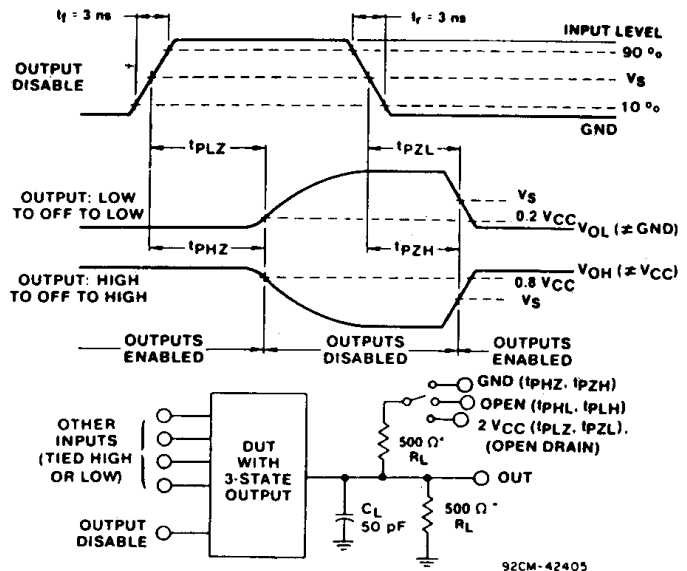
PARAMETER MEASUREMENT INFORMATION



NOTES:

1. V_{OHV} AND V_{OLP} ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:
PRR \leq 1 MHz, $t_r = 3$ ns, $t_f = 3$ ns, SKEW 1 ns.
3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 μ F CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42406

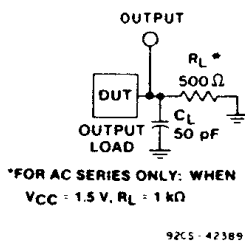


92CM-42405

*FOR AC SERIES ONLY: WHEN $V_{CC} = 1.5$ V, $R_L = 1$ k Ω

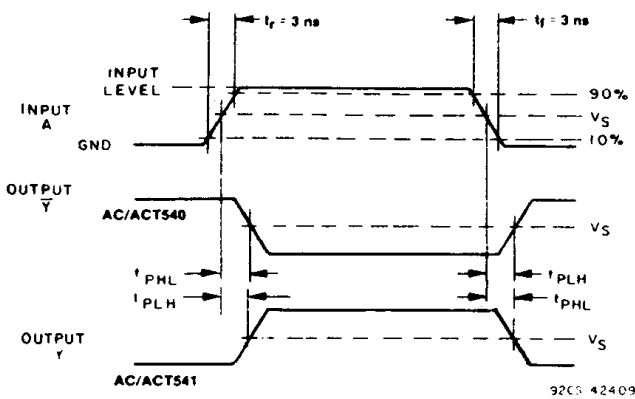
Fig. 1 - Simultaneous switching transient waveforms.

Fig. 2 - Three-state propagation delay waveforms and test circuit.



*FOR AC SERIES ONLY: WHEN $V_{CC} = 1.5$ V, $R_L = 1$ k Ω

92CS-42389



92CS-42409

Fig. 3 - Propagation delay times and test circuit.

	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_s	$0.5 V_{CC}$	1.5 V
Output Switching Voltage, V_s	$0.5 V_{CC}$	$0.5 V_{CC}$

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD54AC541F3A	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
CD54ACT540F3A	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
CD54ACT541F3A	ACTIVE	CDIP	J	20	1	TBD	A42 SNPB	N / A for Pkg Type
CD74AC540M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC540ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC540MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC541E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74AC541EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74AC541M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC541M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC541M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC541M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC541ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC541MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC541SM	OBSOLETE	SSOP	DB	20		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC541SM96	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC541SM96E4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74AC541SM96G4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT540E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74ACT540EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74ACT540M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT540M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT540M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT540M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT540ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT540MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CD74ACT541E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74ACT541EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD74ACT541M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT541M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT541M96E4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT541M96G4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT541ME4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT541MG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT541SM	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
CD74ACT541SM96	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT541SM96E4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD74ACT541SM96G4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC541M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74AC541SM96	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
CD74ACT540M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74ACT541M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
CD74ACT541SM96	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC541M96	SOIC	DW	20	2000	346.0	346.0	41.0
CD74AC541SM96	SSOP	DB	20	2000	346.0	346.0	33.0
CD74ACT540M96	SOIC	DW	20	2000	346.0	346.0	41.0
CD74ACT541M96	SOIC	DW	20	2000	346.0	346.0	41.0
CD74ACT541SM96	SSOP	DB	20	2000	346.0	346.0	33.0

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated